

FIG. 1

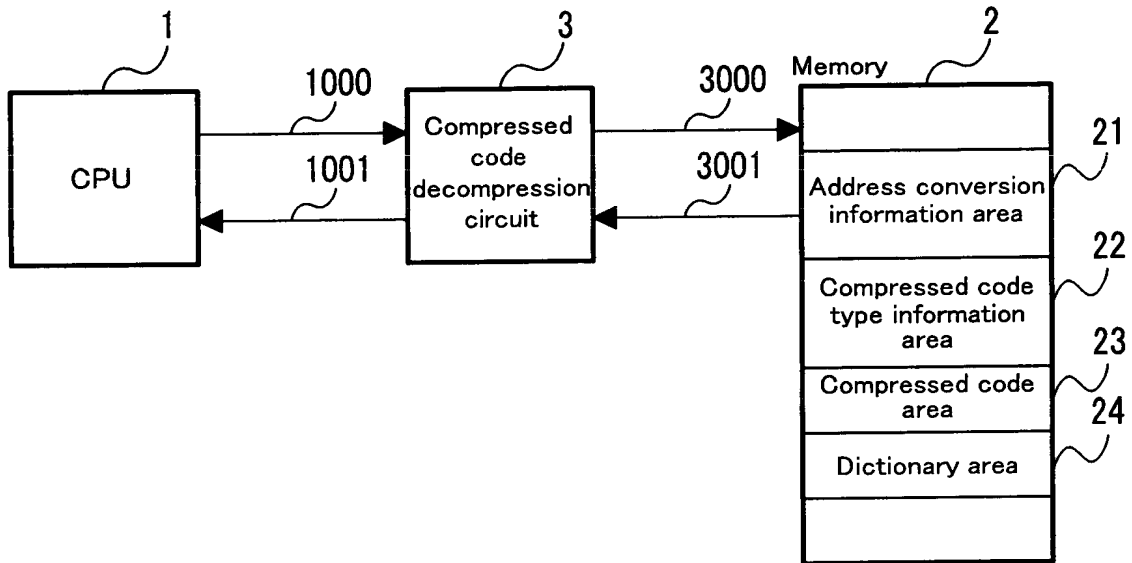


FIG.2A

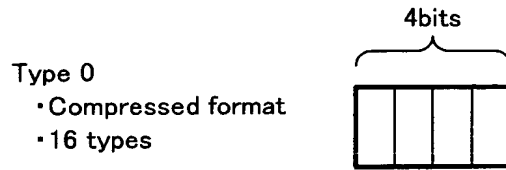


FIG.2B

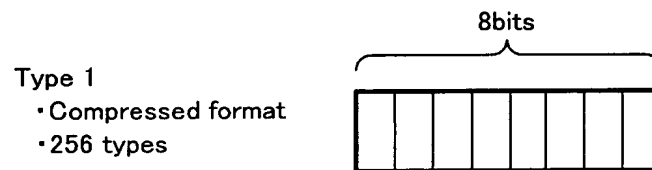


FIG.2C

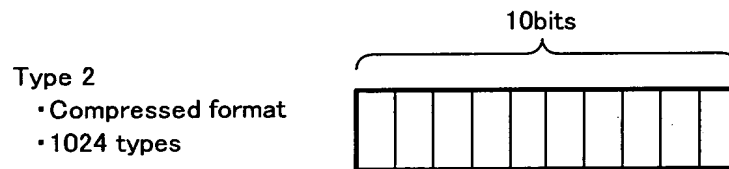


FIG.2D



FIG.3A

FIG.3B

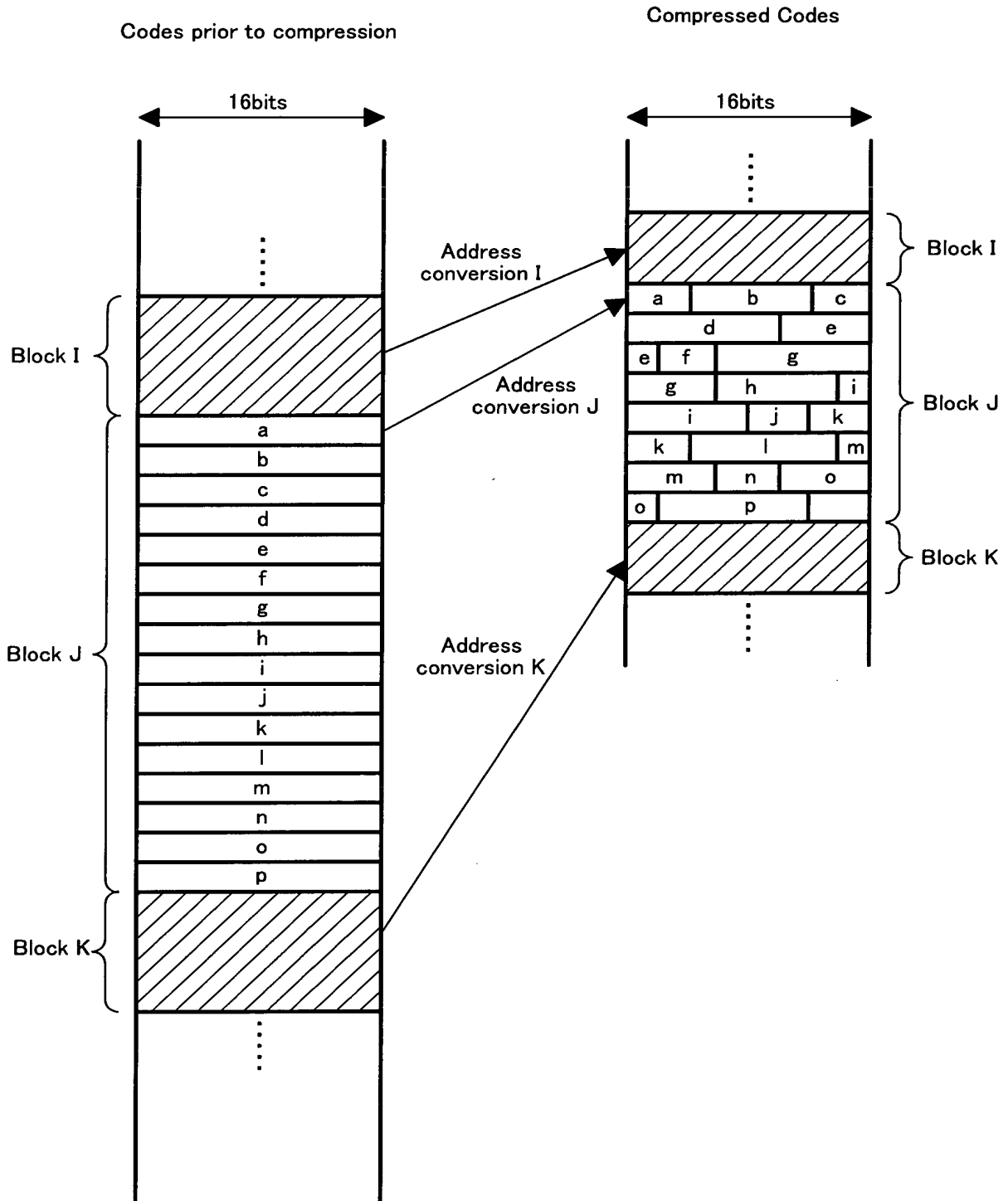


FIG.4A

Codes prior to compression

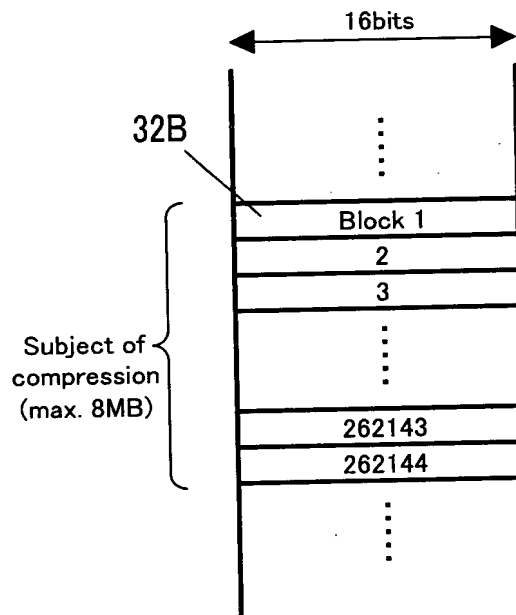


FIG.4B

Address conversion information

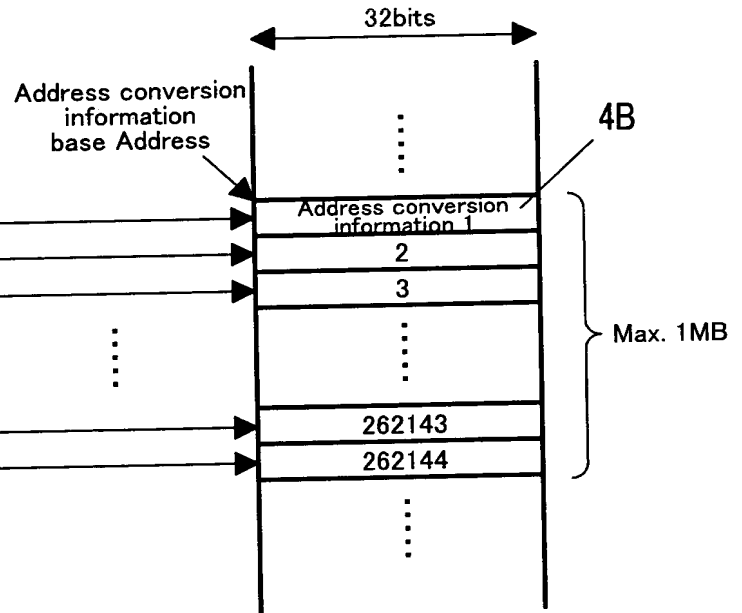


FIG.5

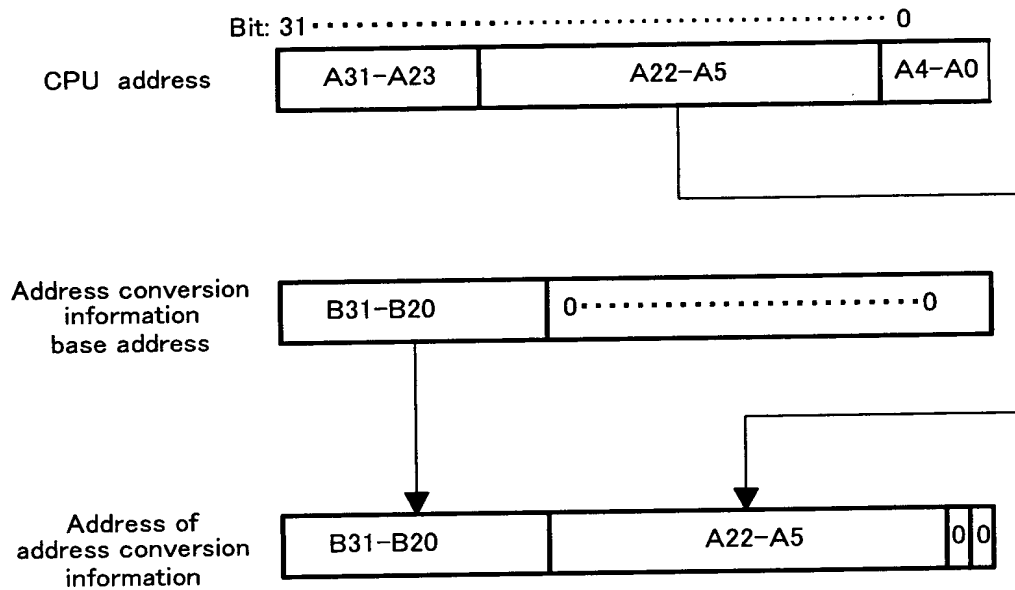


FIG.6

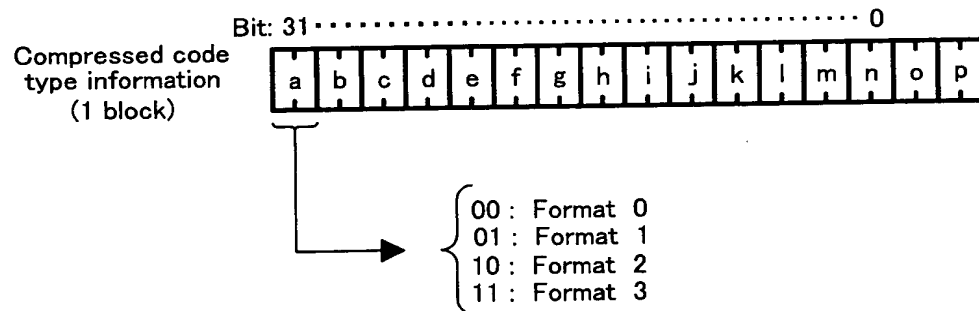


FIG.7A

Codes prior to compression

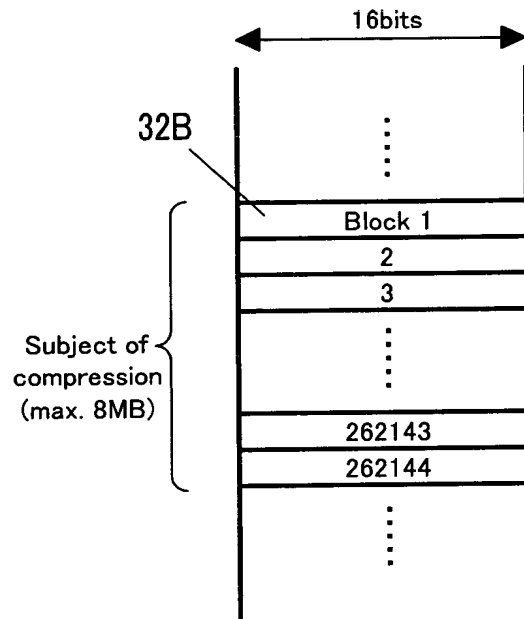


FIG.7B

Compressed code type information

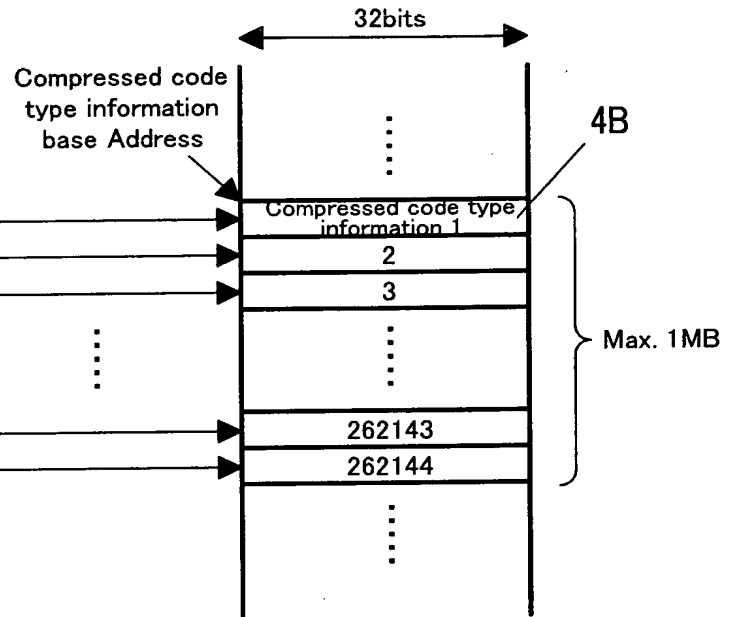


FIG.8

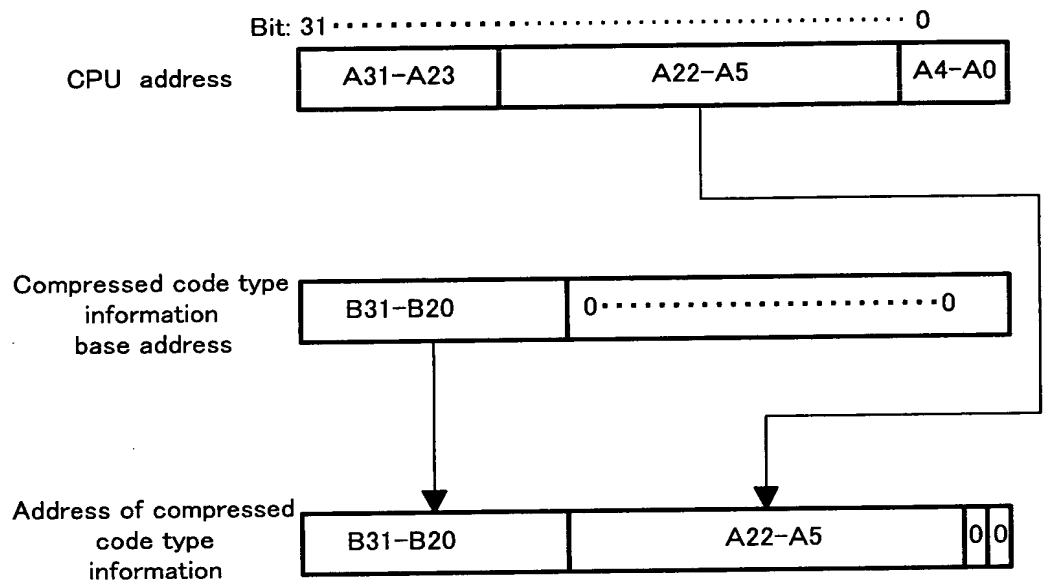


FIG. 9

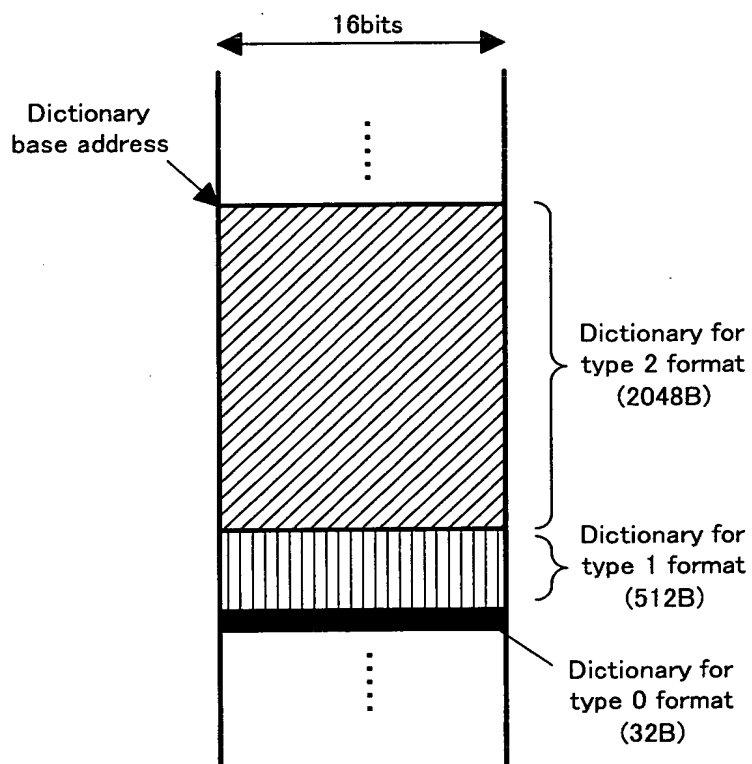




FIG. 11

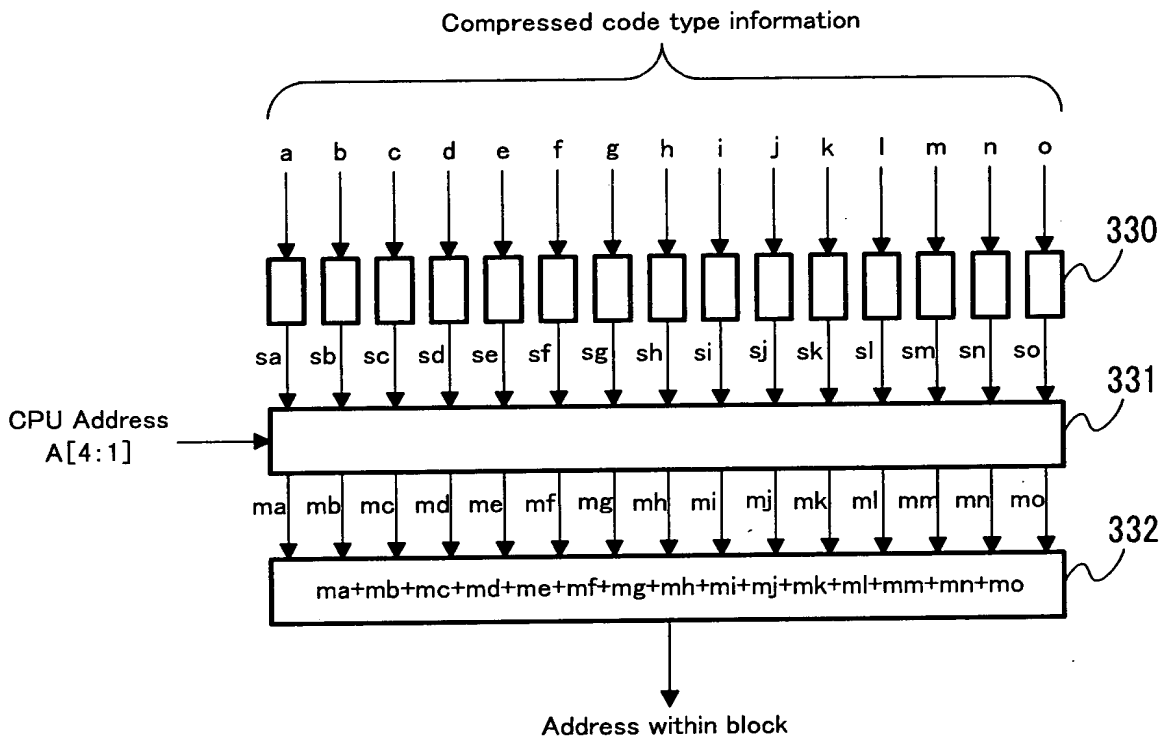


FIG. 12

Input i	Output o
00	0010
01	0100
10	0101
11	1000

FIG. 13

A[4:1]	ma	mb	mc	md	me	mf	mg	mh	mi	mj	mk	ml	mm	mn	mo
0000	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
0001	sa	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
0010	sa	sb	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
0011	sa	sb	sc	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
0100	sa	sb	sc	sd	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
0101	sa	sb	sc	sd	se	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
0110	sa	sb	sc	sd	se	sf	Z	Z	Z	Z	Z	Z	Z	Z	Z
0111	sa	sb	sc	sd	se	sf	sg	Z	Z	Z	Z	Z	Z	Z	Z
1000	sa	sb	sc	sd	se	sf	sg	sh	Z	Z	Z	Z	Z	Z	Z
1001	sa	sb	sc	sd	se	sf	sg	sh	si	Z	Z	Z	Z	Z	Z
1010	sa	sb	sc	sd	se	sf	sg	sh	si	sj	Z	Z	Z	Z	Z
1011	sa	sb	sc	sd	se	sf	sg	sh	si	sj	sk	Z	Z	Z	Z
1100	sa	sb	sc	sd	se	sf	sg	sh	si	sj	sk	sl	Z	Z	Z
1101	sa	sb	sc	sd	se	sf	sg	sh	si	sj	sk	sl	sm	Z	Z
1110	sa	sb	sc	sd	se	sf	sg	sh	si	sj	sk	sl	sm	sn	Z
1111	sa	sb	sc	sd	se	sf	sg	sh	si	sj	sk	sl	sm	sn	so

FIG. 14

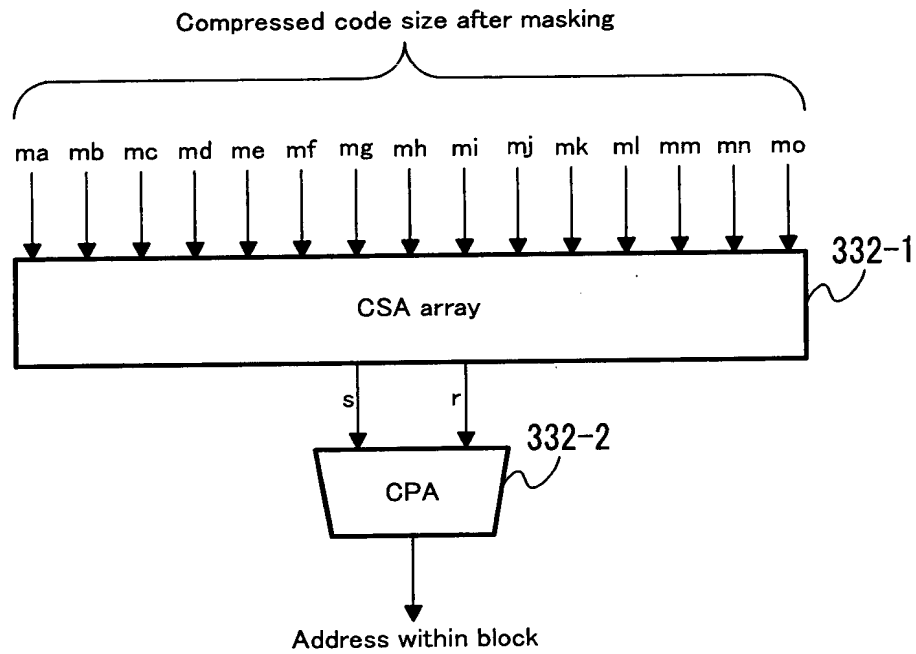


FIG. 15

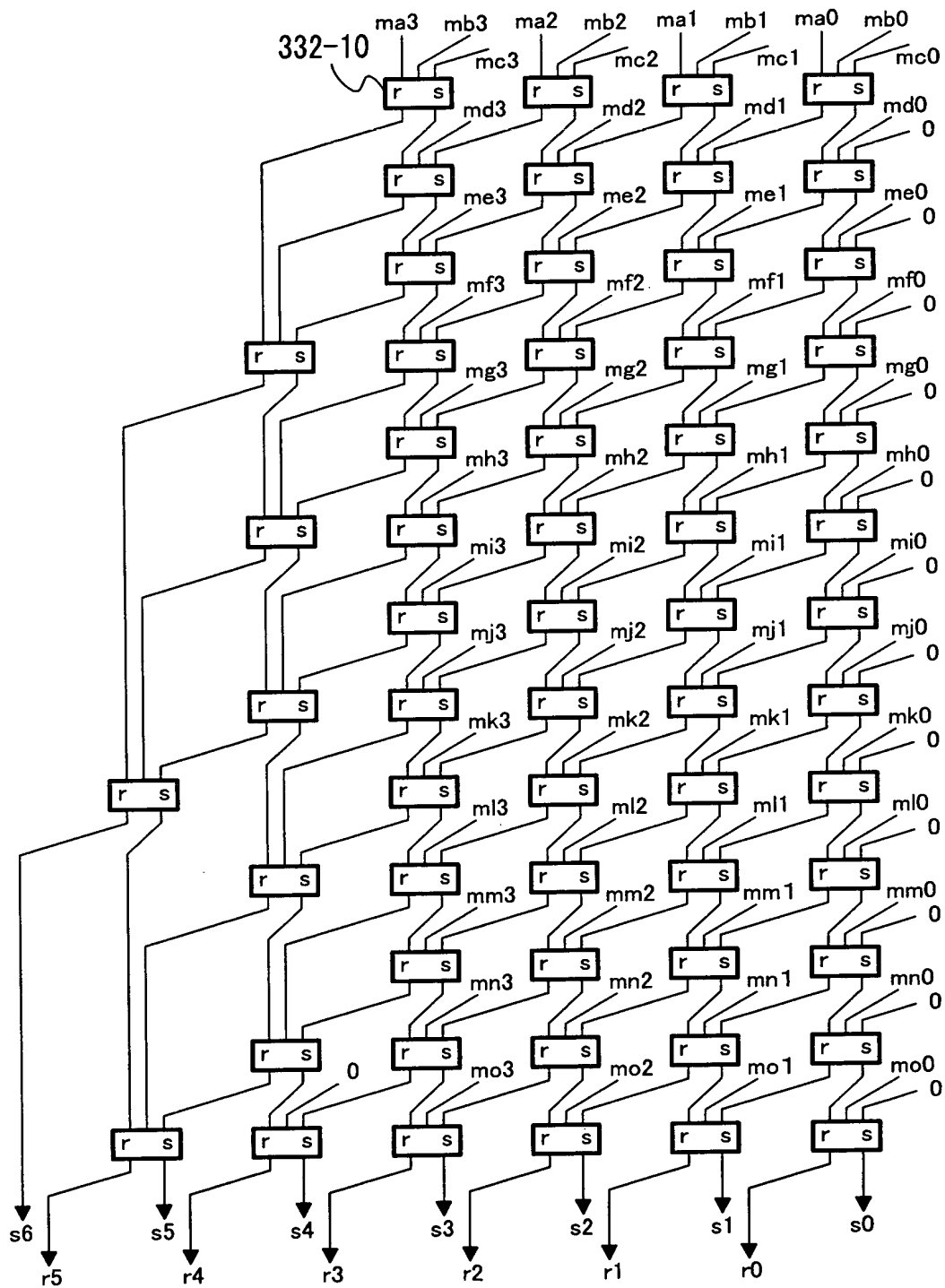


FIG. 16

i0	i1	i2	r	s
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

FIG.17A

Address conversion information
 (head address of compressed code block)

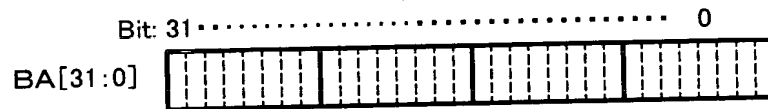


FIG.17B

Address within block

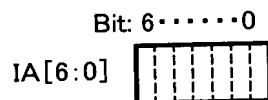


FIG.17C

Compressed code Address

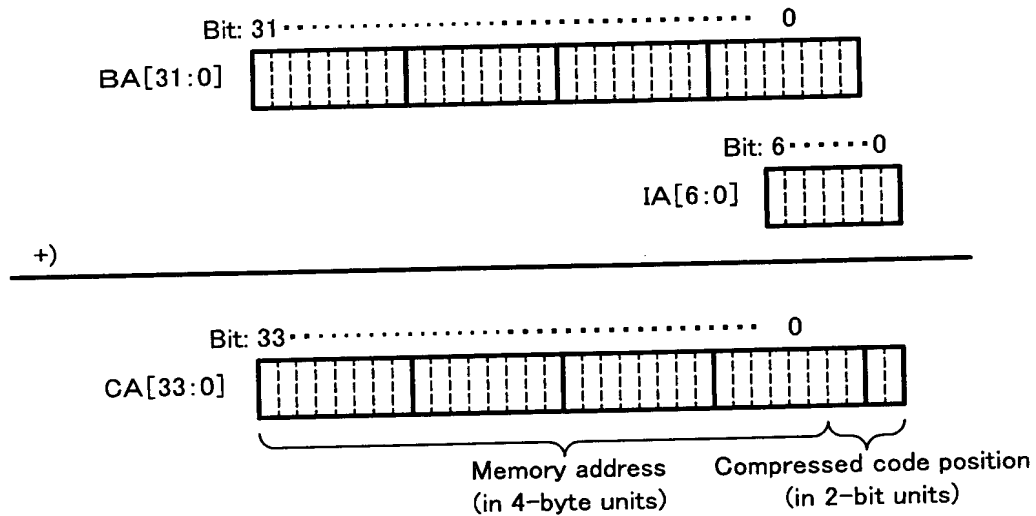


FIG.18

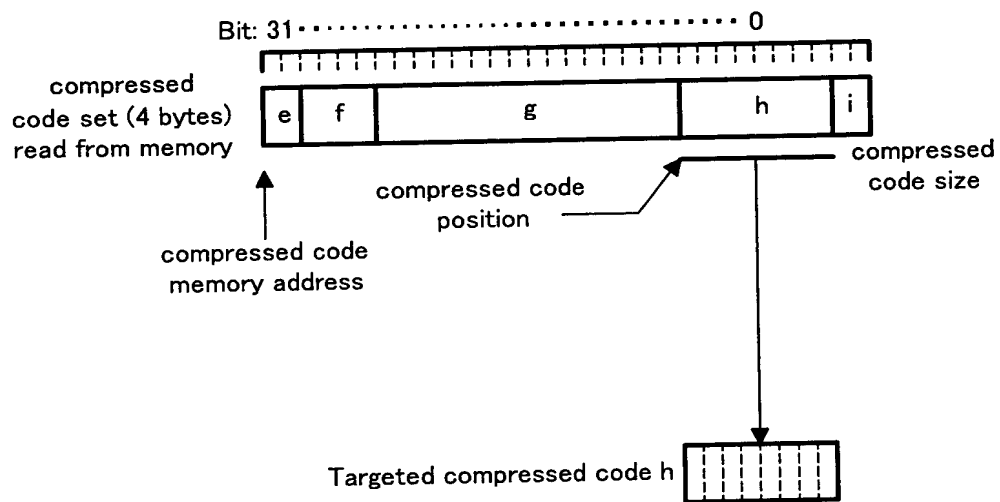


FIG. 19

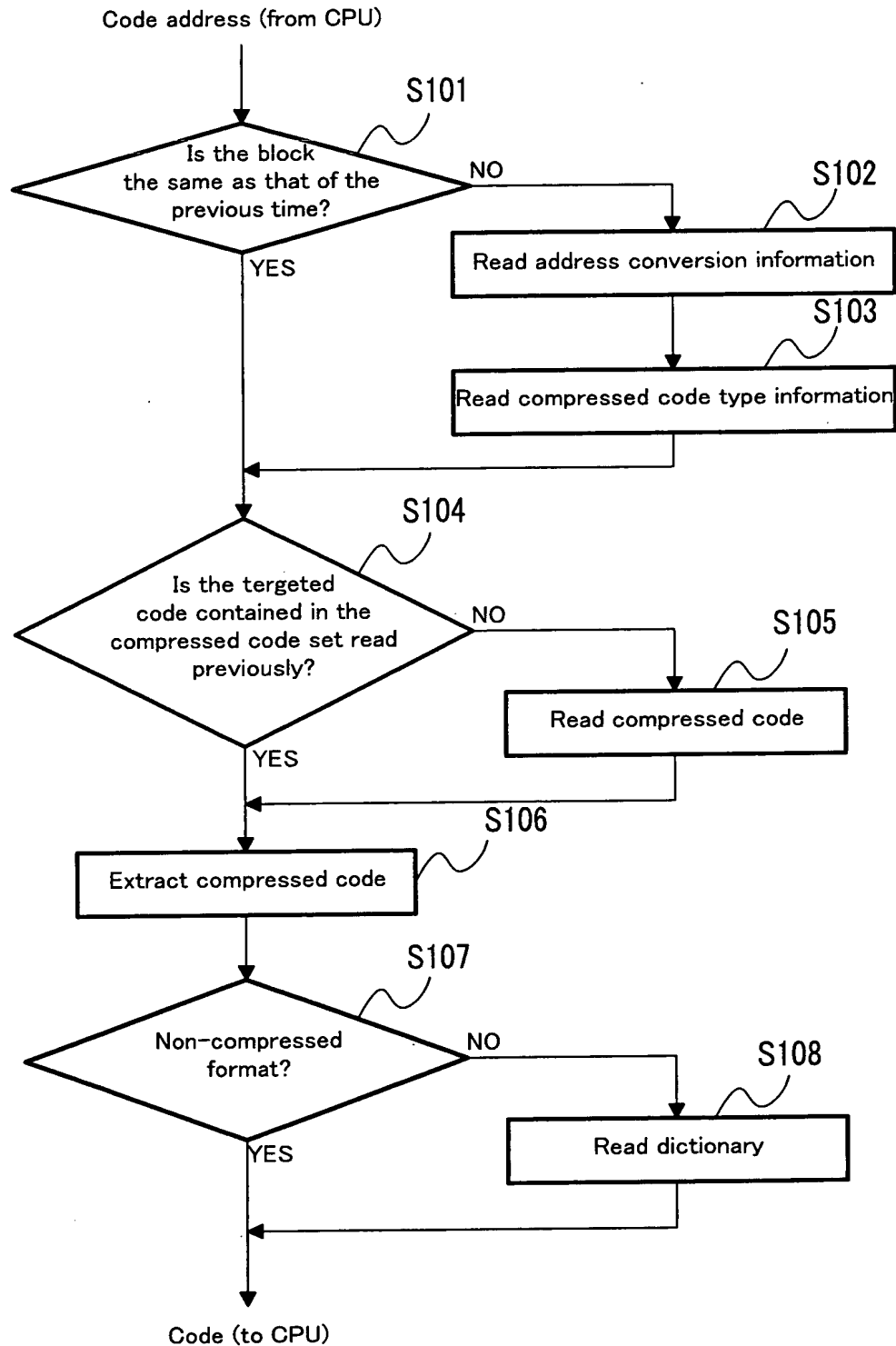


FIG.20

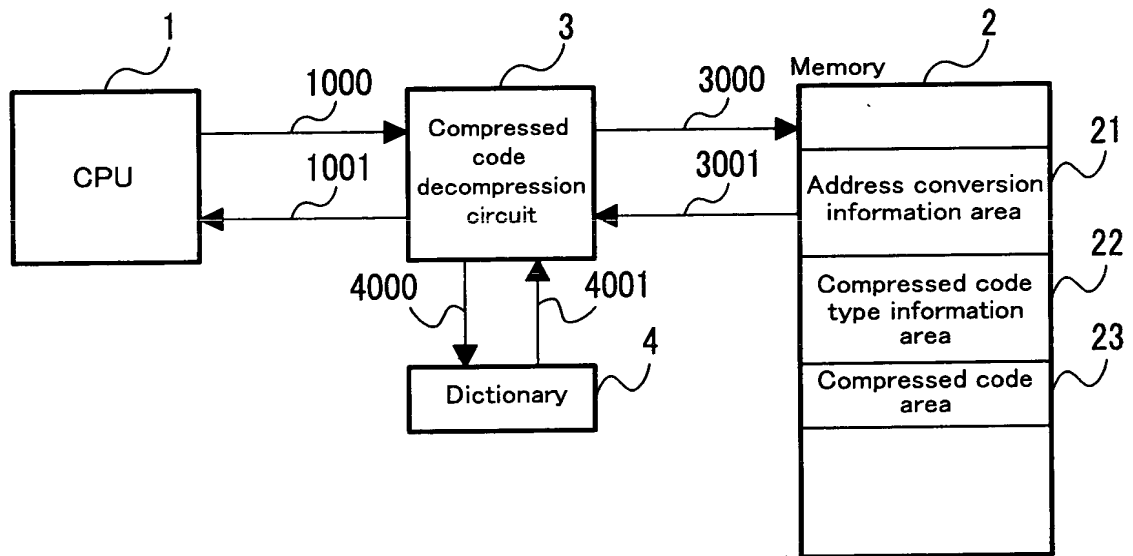


FIG.21

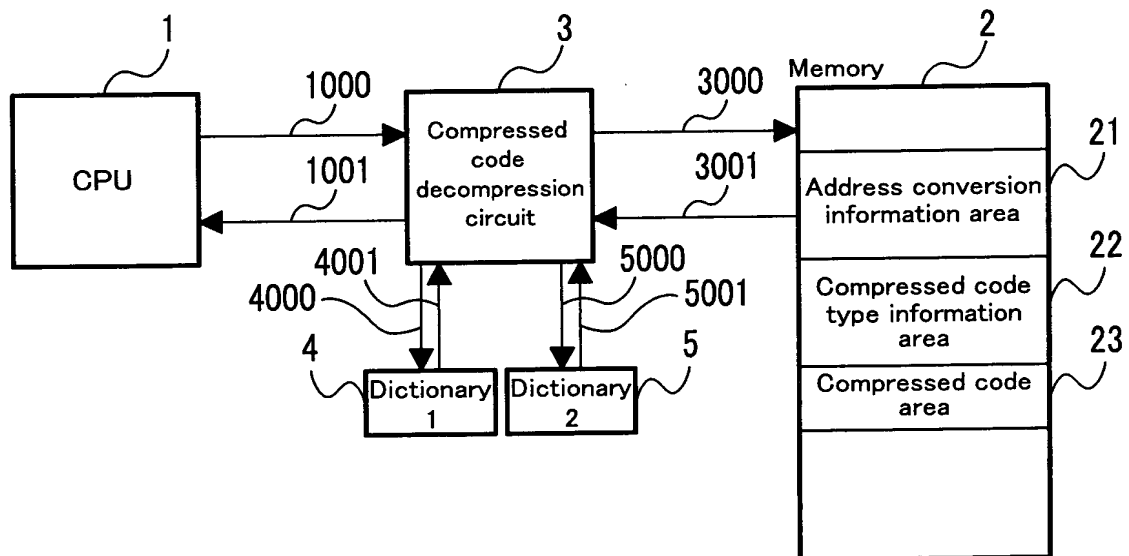


FIG.22

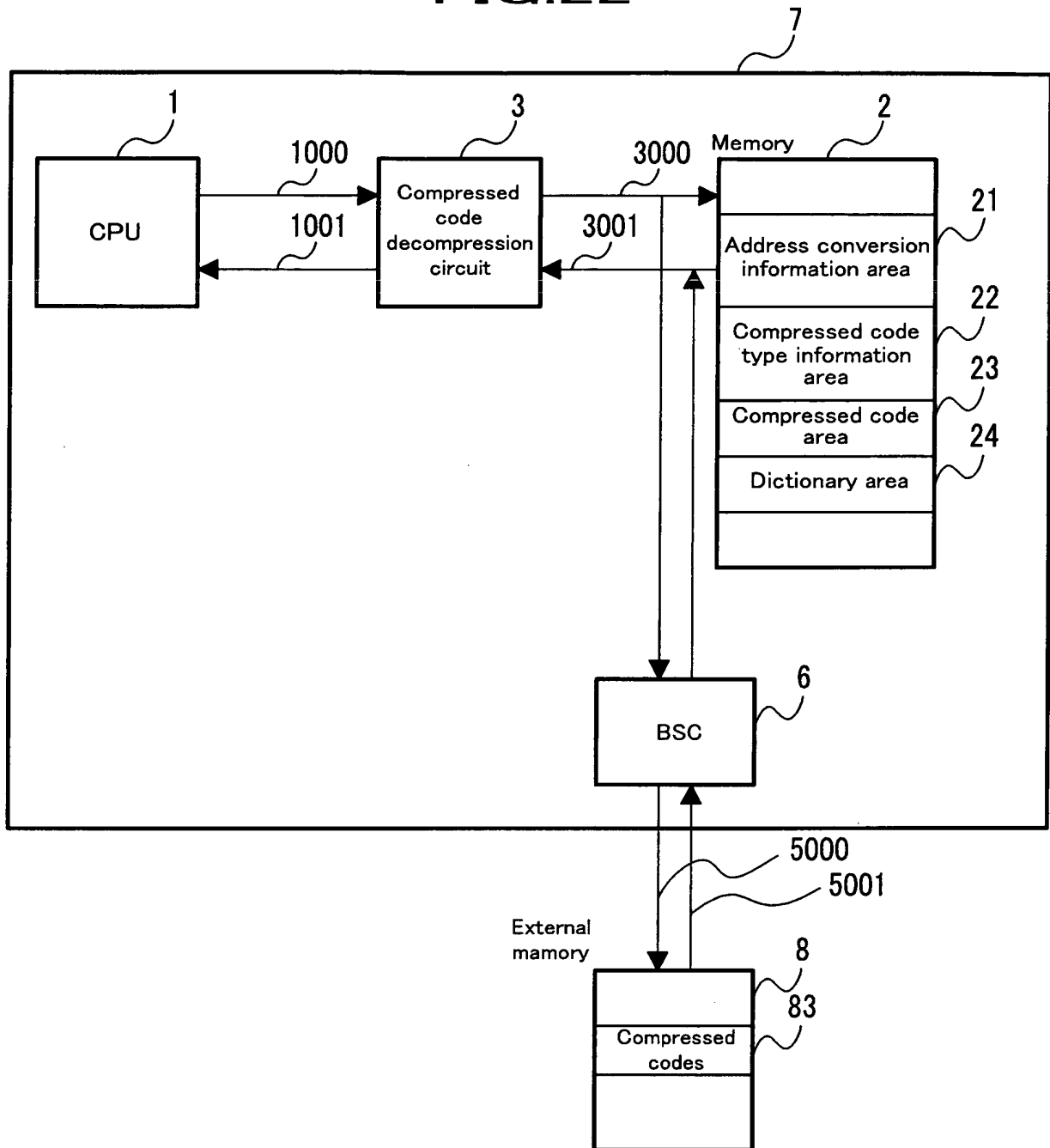


FIG.23

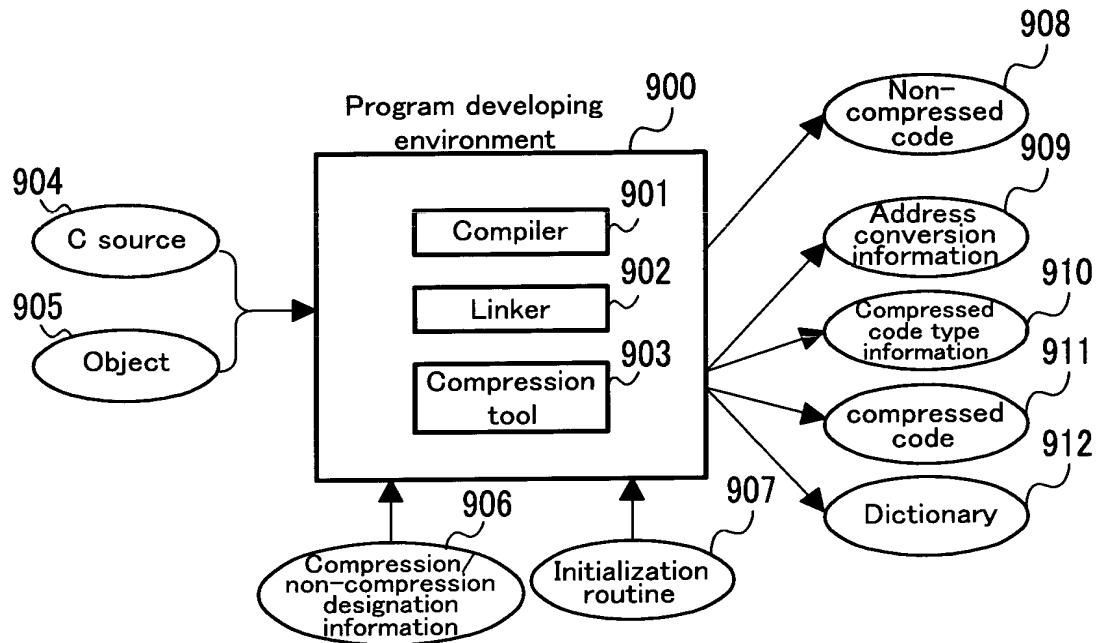


FIG.24

